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BAND-GAP REFERENCE CIRCUIT WITH HIGH POWER SUPPLY RIPPLE REJECTION RATIO

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BACKGROUND

Field of Invention

[0001] The present invention relates to band-gap reference circuits and in particular to low supply voltage, low spreading and high Power Supply Ripple Rejection Ratio band-gap reference circuits.

Description of Related Art

[0002] Band-gap reference circuits provide a voltage essentially independent from the operating temperature, supply voltage, and output current. The temperature dependence of transistor characteristics is detrimental to this design goal. In particular, V_{be} , the base-emitter voltage of bipolar junction transistors typically has a negative temperature coefficient, or “tempco”. This means that the derivative of V_{be} with respect to the temperature, T is negative: $dV_{be}/dT < 0$. This negative tempco can be compensated by creating an output voltage, which is the sum of V_{be} and a compensating V_{pt} voltage:

$$V_{bg} = V_{be} + V_{pt} \quad (1)$$

[0003] Here V_{be} is the emitter-base voltage of the forward biased bipolar transistor junction, and V_{pt} is the PTAT (Proportional To Absolute Temperature) voltage. Visibly, if a V_{pt} is generated with a temperature coefficient, which is equal in magnitude to the negative tempco of V_{be} , but opposite in sign, the sum of these two voltages becomes essentially temperature independent. Since this temperature-independence is achieved by applying voltages close to the band-gap of silicon, these circuits are often termed “band-gap” reference circuits. Correspondingly, the sum of the two voltages is denoted by V_{bg} .

[0004] The dependence of the band-gap reference voltage on the supply voltage is characterized by the ripple rejection ratio. The higher the ripple rejection ratio, the weaker the dependence on the supply voltage.

[0005] The dependence of the band-gap reference voltage on the load, or output current, is characterized by the load dependence, or loop gain. The higher the loop gain, the weaker the dependence on the load.

[0006] Existing designs of band-gap reference circuits either require a high supply voltage for proper operation, or if they operate at low supply voltages such as 1.3-1.4V, the ripple rejection ratio or load gain of these circuits is limited to the range of about 30dB to 40dB

SUMMARY

[0007] Briefly and generally, embodiments of the invention include a band-gap reference circuit with a high Power Supply Ripple Rejection Ratio.

[0008] In some embodiments a band-gap reference circuit includes a core reference circuit with a core output terminal, a voltage amplifier, coupled to the core output terminal and having a voltage amplifier terminal, a transconductance amplifier, coupled to the voltage amplifier terminal, and a shared voltage rail, coupled to the core reference circuit and the transconductance amplifier. The voltage amplifier and the transconductance amplifier can include multiple stages.

[0009] The reference circuit can be operated at low voltages, for example at 1.3-1.4V.

[0010] The reference circuit has low spreading among similarly manufactured systems. This small spreading is partially due to the fact that embodiments of the reference circuit do not utilize differential amplifiers.

[0011] The reference circuit has high power supply ripple rejection ratio. In some embodiments more than 100dB ratios are achieved at low frequencies. Another aspect of the reference circuit is that no startup circuit is required for its operation.

BRIEF DESCRIPTION OF DRAWINGS

[0012] For a more complete understanding of the present invention and for further features and advantages, reference is now made to the following description taken in conjunction with the accompanying drawings.

[0013] FIG. 1 is a block diagram of a band-gap reference circuit according to an embodiment of the invention.

[0014] FIG. 2 illustrates a band-reference circuit according to an embodiment of the invention.

[0015] FIGs. 3A-D illustrate embodiments of a transconductance amplifier, according to embodiments of the invention.

[0016] FIGs. 4A-B illustrate embodiments of a voltage amplifier, according to embodiments of the invention.

[0017] FIG. 5 illustrates a band-reference circuit according to an embodiment of the invention.

[0018] FIG. 6 illustrates a band-reference circuit according to an embodiment of the invention.

[0019] FIGs. 7A-B illustrate embodiments of a voltage amplifier, according to embodiments of the invention.

[0020] FIGs. 8A-D illustrate embodiments of a transconductance amplifier, according

to embodiments of the invention.

DETAILED DESCRIPTION

[0021] Embodiments of the present invention and their advantages are best understood by referring to FIGS. 1-8 of the drawings. Like numerals are used for like and corresponding parts of the various drawings.

[0022] FIG. 1 is a block diagram of a band-gap reference circuit 100 according to some embodiments of the invention. Reference circuit 100 includes a core circuit 1 coupled to a voltage amplifier 2. Voltage amplifier 2 is coupled to a transconductance amplifier 3. The output of reference circuit 100 is coupled back to core circuit 1 through a feedback loop 130.

[0023] FIG. 2 illustrates an embodiment of reference circuit 100. Core circuit 1 includes a current mirror of two transistors Q1 and Q2. Reference circuit 100 will be described in terms of npn transistors. However, alternative designs utilizing pnp, CMOS, and other types of transistors are also meant to be within the scope of the invention. The emitter of transistor Q1 is coupled to the ground. The base of transistor Q1 is coupled to the base of transistor Q2. The base of transistor Q1 is also coupled to the collector of transistor Q1. The collector of transistor Q1 is coupled to voltage rail 112 through resistor R1. The voltage of voltage rail 112 is denoted by V_{bg} for “band gap” voltage. The collector current of transistor Q1 is denoted by I_1 .

[0024] The emitter of transistor Q2 is coupled to the ground through resistor R3. The base of transistor Q2 is coupled to the base of transistor Q1. The collector of transistor Q2 is coupled to voltage rail 112 through resistor R2. A core voltage terminal 115 is also coupled to the collector of transistor Q2. The collector current of transistor Q2 is denoted by I_2 .

[0025] One of the roles of the current mirror is to generate a positive tempco voltage V_{pt} . In particular, transistor Q2 produces an emitter current with a positive temperature coefficient as described below. This positive tempco current is translated into a positive tempco voltage V_{pt} by inserting resistor R2 into the collector circuit of transistor Q2.

[0026] In general, the temperature and current dependence of a base-emitter voltage V_{be} is described by the Ebers-Moll equation:

$$V_{be} = V_T [\ln(I_c/I_s) + 1] \quad , \quad (1)$$

[0027] where $V_T = kT/q$ is the “thermal voltage”. Here k is Boltzmann’s constant, q is the magnitude of the electron charge, I_c is the collector current, and I_s is the saturation current. Using the Ebers-Moll equation in the so-called logarithmic calculus shows that the PTAT voltage V_{pt} across resistor R_2 is given by:

$$V_{pt} = (R_2/R_3) * (kT/q) * \ln(I_{c2}/I_{c1}) \quad . \quad (2)$$

[0028] Visibly, V_{pt} grows with the temperature, therefore, it has a positive temperature coefficient. The leading temperature dependence of the V_{pt} voltage is linear with possible logarithmic corrections. In some circuits the closed loop gain $K = R_2/R_3$ is controlled into the range of 4-8. In other circuits K can assume considerably higher values, up to a hundred.

[0029] In some designs transistors Q_1 and Q_2 are essentially identical, but the currents I_{c1} and I_{c2} can be different, with I_{c1} typically larger than I_{c2} .

[0030] In other designs currents I_{c1} and I_{c2} are essentially equal and transistors Q_1 and Q_2 have different sizes. In some designs the area ratio M of Q_2 relative to Q_1 is between about 4 to about 100. In some embodiments the area ratio can be any value. Alternatively, transistor Q_2 can be made up by a plurality of similar or essentially identical transistors coupled in parallel.

[0031] Core circuit 1 is coupled to voltage amplifier 2. Voltage amplifier 2 includes operational amplifier, or opamp 125. In some embodiments opamp 125 includes a bipolar junction transistor Q_4 as an input stage. The input terminal of opamp 125, which can be the base of transistor Q_4 , is coupled to core voltage terminal 115. The emitter of transistor Q_4 is coupled to the ground. Voltage rail 112 provides voltage for opamp 125. Opamp 125 also has a voltage amplifier terminal 133. The supply current of opamp 125 is denoted as I_a .

[0032] Voltage amplifier 2 is coupled to transconductance amplifier 3.

Transconductance amplifier 3 includes transistor Q_3 . The base of transistor Q_3 is

coupled to voltage amplifier terminal 133. The emitter of transistor Q3 is coupled to the ground. The collector of transistor Q3 is coupled to voltage rail 112. The collector current of transistor Q3 is denoted by I3.

[0033] Voltage rail 112, serving as the output of band-gap reference circuit 100, is coupled to load 173, represented by resistor Rload. Therefore, the Vbg voltage of voltage rail 112 is applied across Rload, generating a current Iload across Rload.

[0034] Band-gap reference circuit 100 is driven by voltage generator 181, which generates supply voltage Vs. Voltage generator 181 drives reference circuit 100 through current generator 192. Current generator 192 is operable to limit the current, drawn from voltage generator 181.

[0035] The feedback action of feedback loop 130 is provided by coupling the band gap voltage Vbg into voltage rail 112.

[0036] Next, the operation of reference circuit 100 will be described. In core circuit 1 the base and collector of transistor Q1 are coupled together, therefore the collector voltage of transistor Q1 is equal to a diode drop. Thus, for a given Vbg the value of I1, the collector current of transistor Q1, is determined by resistor R1. The value of I2, the collector current of transistor Q2, is determined by I1, R3, and M, the area – ratio of transistors Q2 and Q1. Logarithmic calculus yields:

$$I2 = (1/R3)*(kT/q)*\ln(M*I1/I2) \quad . \quad (3)$$

[0037] The voltage drop across resistor R2 is the PTAT voltage Vpt:

$$Vpt = (R2/R3)*(kT/q)*\ln(M*I1/I2) \quad . \quad (4)$$

[0038] Since the emitter of transistor Q4 is coupled to the ground, a Vbe voltage appears at the base of transistor Q4. Core voltage terminal 115 transfers this Vbe voltage to the collector of transistor Q2. Since Vpt is the voltage drop across resistor R2, the voltage Vbg of voltage rail 112 equals the sum of Vbe and Vpt:

$$Vbg = Vpt + Vbe$$

[0039] Vbe is proportional to the temperature with a negative temperature coefficient and Vpt is proportional to the temperature with a positive temperature coefficient.

Therefore, an appropriate choice of the parameters R2, R3, and M can create a positive tempco Vpt, which is capable of fully compensating the negative tempco of Vbe, resulting in a Vbg, which is essentially temperature independent.

[0040] Embodiments of the invention do not use differential amplifiers. Differential amplifiers have offsets because of the mismatch of the parameters of their transistors, and hence increase spreading. Here “spreading” refers to the variation of the band-gap voltage of a batch of manufactured circuits.

[0041] Embodiments of the invention operate at low voltage supplies. The operating voltage supply can be in the range of about 0.6V to about 3V, for example, about 1.3V. For low supply voltages, such as 1.3V, existing operational amplifiers do not have sufficient headroom. Therefore, the gain of existing low supply voltage amplifiers is low. Typically, the ripple rejection ratio is proportional to the gain, thus, the ripple rejection ratio of existing low voltage amplifiers is also low. In some existing low voltage amplifiers the ripple rejection ratio is in the range of 30dB – 40dB.

[0042] In contrast, embodiments of the present invention can reach ripple rejection ratios of about 100dB, as demonstrated below.

[0043] The ripple rejection ratio is determined by the differential response of reference circuit 100 to small changes in the supply voltage. The load dependence is characterized by the differential response of the band-gap voltage to small changes in the output current. These responses will be characterized by the ratios dV_{bg}/dV_s and dV_{bg}/dI_{load} . The first part of the analysis does not incorporate the effect of voltage amplifier 2

[0044] If the supply voltage V_s , provided by voltage generator 181, changes by a small amount of dV_s , the current I_s of current source 192 changes by the corresponding small amount of dI_s . The rate of this change can be expressed through R_s , the internal differential resistance of current generator I_s , as:

$$R_s = dV_s / dI_s \quad . \quad (5)$$

[0045] Changing I_s by an infinitesimal value dI_s causes a dV_{bg} change in V_{bg} , a dI_1 change in I_1 , a dI_2 change in I_2 , a dI_3 change in I_3 , and a dI_{load} change in I_{load} . To a

good approximation

$$dI_1 = dV_{bg} / R_1 ; \quad dI_2 = 0 ; \quad (6)$$

$$dI_3 = g_{m3} * dV_{bg} ; \quad dI_{load} = dV_{bg} / R_{load}$$

[0046] where g_{m3} is the transconductance of transistor Q3.

[0047] Applying Kirchhoff's first law to current node 194 yields:

$$dI_s = dI_1 + dI_2 + dI_3 + dI_{load} \quad (7)$$

[0048] From Equations (5), (6) and (7) the change in V_{bg} caused by the change in supply voltage V_s is:

$$dV_{bg}/dV_s = 1/[R_s*(1/R_1+1/R_{load}+g_{m3})] \sim 1/[R_s*g_{m3}] \quad (8)$$

[0049] where the last approximation holds for systems in which g_{m3} is much larger than $1/R_1$ and $1/R_{load}$. This ratio captures the change dV_{bg} of the band-gap voltage V_{bg} in response to a change dV_s in the supply voltage V_s .

[0050] Next, the change dV_{bg} of the band gap voltage V_{bg} in response to a dI_{load} change of the load current I_{load} will be calculated. For example, I_{load} can change for some external reason, in which case dI_{load} may cease being equal to dV_{bg}/R_{load} . In these situations the operating current I_s of current source 192 does not change (i.e. $dI_s=0$). Then equations (6) and (7) yield for the dV_{bg} / dI_{load} ratio:

$$dV_{bg} / dI_{load} = - 1 / (1/R_1 + g_{m3}) \sim - 1 / g_{m3} \quad (9)$$

[0051] In summary, the differential responses of the band-gap voltage V_{bg} due to changes in the supply voltage V_s and load current I_{load} are captured by equations (8) and (9). These differential responses determine the ripple rejection ratio and load dependence of reference circuit 100. As equations (8) and (9) demonstrate, the differential responses are primarily determined by g_{m3} , the transconductance of transconductance amplifier 3.

[0052] The higher the transconductance g_{m3} , the smaller the changes in band-gap

voltage V_{bg} in response to changes in the supply voltage V_s or the load current I_{load} .

[0053] The described embodiments of band-gap reference circuit 100 among others have the following aspects. They operate at low supply voltages, in the range of about 0.6 V to about 3V, for example about 1.3 – 1.4 V. The spreading of band-gap voltage V_{bg} from system to system is low, caused only by a mismatch of the parameters of transistors Q1 and Q2 and resistors R2 and R3. Also, band-gap reference circuit 100 has a simple layout and requires no start-up circuit.

[0054] However, the ripple rejection ratio of embodiments without a voltage amplifier is limited by the value of gm_3 . Typical values of the ripple rejection ratio in these embodiments are in the range of about 30 dB to 40dB.

[0055] Next, the effect of including voltage amplifier 2 will be described. In general, these embodiments also operate at low supply voltages, have a simple layout, and preserve the low spreading of V_{bg} . In addition, however, they provide an improvement in the ripple rejection ratio.

[0056] The voltage gain of voltage amplifier 2 is defined as: $A_u = V_{out}/V_{in}$. Some aspects of voltage amplifier 2 include the following. The input voltage V_{in} and output voltage V_{out} have essentially the same phase. Also, the voltage gain $A_u = V_{out}/V_{in}$ of voltage amplifier 2 is much larger than one. Further, voltage amplifier 2 is biased from the band-gap voltage V_{bg} or some other constant voltage source.

[0057] Finally, the input stage of voltage amplifier 2 includes npn bipolar transistor Q4, coupled to the emitter base junction of Q3. As described above, in this way the band gap voltage V_{bg} , which is the sum of PTAT voltage V_{pt} across resistor R2, and the emitter base voltage V_{be} of bipolar transistor Q4, will be essentially independent of the temperature.

[0058] Voltage amplifier 2 enhances the band-gap voltage power supply ripple rejection ratio as described below.

[0059] When supply voltage V_s changes by an amount dV_s , the current of current source 192 changes by dI_s , given by

$$R_s = dV_s / dI_s \quad . \quad (11)$$

[0060] Here R_s is the internal resistance of current generator I_s .

[0061] The change dI_s causes a change in V_{bg} (dV_{bg}) and in the currents I_1 (dI_1), I_2 (dI_2), I_a (dI_a), I_3 (dI_3), and I_{load} (dI_{load}). According Kirchoff's first law as applied to node 194

$$dI_s = dI_1 + dI_2 + dI_a + dI_3 + dI_{load} \quad (12)$$

[0062] where

$$dI_1 = dV_{bg} / (R_1 + 1/gm_1) = dV_{bg} / R_1 \quad (13)$$

$$dI_2 = 1/R_3 * kT/q * dI_1/I_1 = 1/gm_1/R_3 * dI_1 \ll dI_1 \quad (14)$$

[0063] and therefore

$$dV_{bg} = dV_{in} \quad (15)$$

$$dI_a \ll dI_3 \quad (16)$$

$$dI_3 = A_u * gm_3 * dV_{bg} \quad (17)$$

$$dI_{load} = dV_{bg} / R_{load} \quad (18)$$

[0064] From equations (11) and (18) it follows that the change in V_{bg} with respect to change in supply voltage V_s is:

$$dV_{bg} = dV_s / R_s / (1/R_1 + 1/R_{load} + A_u * gm_3) = dV_s / R_s / (A_u * gm_3) \quad (19)$$

[0065] From equation (12) with $dI_s = 0$ and equations (13) – (18) we can obtain the change in V_{bg} in response to a change dI_{load} in load current I_{load} :

$$dV_{bg} / dI_{load} = - 1 / (1/R_1 + A_u * gm_3) = - 1 / (A_u * gm_3) \quad (20)$$

[0066] The comparison of equations (8) and (9) with equations (19) and (20) illustrates that the introduction of voltage amplifier 2 reduces the changes in the band-gap voltage due to changes in either the supply voltage or the load current by the factor of the voltage amplifier gain A_u . With the A_u enhancement factor, embodiments of the invention reach ripple rejection ratios in the range of about 50 dB to about 120 dB, for example about 100dB.

[0067] FIGs. 3A-D illustrate various embodiments of transconductance amplifier 3. FIG. 3A illustrates that transconductance amplifier 3 can be a simple npn transistor with a transconductance: $gm_3 = dI_3/dV_{out} = gm_{npn3}$. Here gm_{npn3} is the transconductance of the bipolar npn Q_{npn3} transistor.

[0068] FIG. 3B illustrates that in other embodiments transconductance amplifier 3 is a two-stage amplifier, including coupled npn and pnp transistors with a transconductance: $gm_3 = dI_3/dV_{out} = gm_{npn3} \times gm_{pnp3} \times (R // h_{iepnp3}) > gm_{npn3}$. Here gm_{pnp3} is the transconductance of the bipolar pnp Q_{pnp3} transistor, and h_{iepnp3} is the small signal input base resistance of transistor Q_{pnp3} .

[0069] FIG. 3C illustrates that in other embodiments transconductance amplifier 3 can be a NMOS transistor with a transconductance: $gm_3 = dI_3/dV_{out} = gm_{nmos3}$. Here gm_{nmos3} is the transconductance of the NMOS Q_{nmos3} transistor.

[0070] FIG. 3D illustrates that in other embodiments transconductance amplifier 3 is a two-stage amplifier, including coupled NMOS and PMOS transistors with a transconductance: $gm_3 = dI_3/dV_{out} = gm_{nmos3} \times gm_{pmos3} \times R > gm_{pmos3}$. Here gm_{pmos3} is the transconductance of the PMOS Q_{pmos3} transistor.

[0071] It can be seen that the transconductance gm_3 has a higher value for the two-stage embodiments of FIG. 3B and FIG. 3D.

[0072] FIGs. 4A and 4B illustrate related embodiments of voltage amplifier 2. Both are two stage amplifiers, including two transistors and two resistors.

[0073] First stage transistor Q_4 is a bipolar npn transistor, which provides the V_{be} voltage at terminal 115, used in generating the band-gap voltage V_{bg} . The second stage transistor Q_5 in FIG. 4A is a bipolar npn transistor, and in FIG. 4B an NMOS transistor.

[0074] The voltage gain A_u for voltage amplifier 2 is:

$$A_u = A_4 \times A_5 = (gm_4 \times R_4) \times (gm_5 \times R_5) \quad (21)$$

[0075] Here A_4 and A_5 are the gains for the first stage (Q_4 , R_4) and second stage (Q_5 , R_5) of voltage amplifier 2.

[0076] The change dI_a in amplifier current I_a in response to a change dV_{bg} in the V_{bg}

voltage can be calculated with the help of equations (15) and (21) as follows :

$$dI_a = dI_4 + dI_5 = g_{m4} dV_{bg} - g_{m5} (g_{m4} R_4) dV_{bg} = - g_{m5} (A_4) dV_{bg} \quad (22)$$

[0077] Equation (22) shows that when V_{bg} increases, and correspondingly dV_{bg} is positive, the amplifier current I_a decreases. This means that the voltage amplifier introduces a positive feedback for band-gap voltage V_{bg} .

[0078] Furthermore, using equation (17) and (22), taking into account that $g_{m3} = g_{m5}$, and that usual values for voltage gain stages are A_4 greater than 10 and A_5 greater than 10, it is seen that

$$dI_3 = g_{m3} A_u dV_{bg} = g_{m3} A_4 A_5 dV_{bg} \gg dI_a = g_{m5} A_4 dV_{bg} \quad (23)$$

[0079] Equation (23) demonstrates that the negative feedback introduced by transconductance amplifier 3 is bigger than the positive feedback introduced by voltage amplifier 2. Therefore, the overall feedback for band-gap reference circuit 100 is appropriate for stable operations.

[0080] Further aspects of reference circuit 100 include that the operating voltage is low. In some embodiments the operating voltage of reference circuit 100 is about 0V to about 0.5V above the band gap voltage, for example about 0.1V – 0.2 V above the band gap voltage.

[0081] Another aspect of reference circuit 100 is the small spread, or, equivalently, tight tolerance of the band-gap voltage V_{bg} from circuit to circuit. This small spread is partially due to the fact that embodiments of reference circuit 100 do not utilize differential amplifiers. In existing circuits the amplifier offset multiplied by the PTAT voltage resistor ratio ($V_{off} * R_2/R_3$) enhances the spreading of the band-gap voltage V_{bg} .

[0082] Another aspect of reference circuit 100 is the high power supply ripple rejection ratio. In some embodiments more than 100dBV ratios are achieved at low frequencies.

[0083] Another aspect of reference circuit 100 a high band gap voltage load regulation.

[0084] Another aspect of reference circuit 100 that the noise is low. This aspect is related to using bipolar transistors as first stages for voltage amplifier 2 and transconductance amplifier 3 in some embodiments.

[0085] Another aspect of reference circuit 100 is that no startup circuit is required for its operation.

[0086] Another aspect of reference circuit 100 is that it requires only a small capacitance for frequency circuit compensation. For example, the relatively small compensation capacitance value of about 3 - 5 pF is sufficient for more than 70 degrees phase margin.

[0087] FIG. 5 illustrates another embodiment of band-gap reference circuit 100 utilizing Bipolar and BiCMOS elements. The overall topology of the circuit is analogous to that FIG. 2 and will not be described in detail.

[0088] The differences relative to FIG. 2 include that voltage amplifier 2 is a two-stage amplifier, containing first stage bipolar transistor Q4 and second stage CMOS transistor M0. Also an additional RC link, including Rc1 and Cc1, has been coupled between the collector and the base of transistor Q4.

[0089] In this embodiment transconductance amplifier 3 is also a two-stage amplifier, containing first stage CMOS transistor M1 and second stage CMOS transistor M2. Also, an additional capacitor Cc2 has been coupled between voltage rail 112 and the gate of CMOS transistor M1.

[0090] In this embodiment the input current does not reach low values. This is due to the fact that PTAT current I2 is higher than the parasitic diode current provided by the collector of transistor Q2. In some embodiments the value of parasitic diode currents at high temperatures, for example about 125 C, can be in the range of tens of nano-Amperes.

[0091] FIG. 6 illustrates an embodiment, complementary to the embodiment of FIG. 2. In this embodiment npn (pnp) transistors are replaced by pnp (nnp) transistors and nmos (pmos) transistors are replaced by pmos (nmos) transistors.

[0092] FIGs. 7A-B illustrate embodiments, complementary to the embodiments of

voltage amplifier 2 in FIGs. 4A-B. In this embodiment npn (pnp) transistors are replaced by pnp (nnp) transistors and nmos (pmos) transistors are replaced by pmos (nmos) transistors.

[0093] FIGs. 8A-D illustrate embodiments, complementary to the embodiments of transconductance amplifier 3 in FIGs. 3A-D. In this embodiment npn (pnp) transistors are replaced by pnp (nnp) transistors and nmos (pmos) transistors are replaced by pmos (nmos) transistors.

[0094] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions, and alterations can be made therein without departing from the spirit and scope of the invention as defined by the appended claims. That is, the discussion included in this application is intended to serve as a basic description. It should be understood that the specific discussion may not explicitly describe all embodiments possible; many alternatives are implicit. It also may not fully explain the generic nature of the invention and may not explicitly show how each feature or element can actually be representative of a broader function or of a great variety of alternative or equivalent elements. Again, these are implicitly included in this disclosure. Where the invention is described in device-oriented terminology, each element of the device implicitly performs a function. Neither the description nor the terminology is intended to limit the scope of the claims.